Post-Enabled Precision Flip-Chip Assembly for Variable MEMS Capacitor

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Abstract **— A variable capacitor array with a high Q-factor and a high tuning ratio is demonstrated. A novel "post-enabled" flip-chip assembly allows precise multiple digital capacitance levels within one device. This capacitor array is realized by a hybrid integration of a MEMS device with RF circuits on an alumina substrate. The MEMS is prefabricated using a commercially available foundry process and is initially suspended using mechanical tethers on a silicon substrate, which is removed during the flip-chip assembly. The precise gap between the MEMS and the RF circuit is controlled using posts. Each post is designed by a stack of structural layers available in the commercial foundry process. We measured a Q-factor above 200 at 1 GHz, a capacitance ratio of 4.7:1, and tuning range of 171 MHz in a resonator circuit. More importantly, we achieved a digital capacitance level and negligible warpage due to the excellent gap control following the flip-chip assembly.**

I. INTRODUCTION

Advances in packaging technology are important to the fabrication of RFMEMS-based devices through existing silicon-based integrated circuit (IC) or MEMS foundry processes. The MUMPs process is an example [1]. It is well known that low-resistively silicon used in IC foundry processes is not a good substrate for RF applications due to its high losses at RF frequencies. Therefore, a flip-chip assembly process with silicon removal technology has been developed to transfer MEMS from the silicon to a ceramic substrate containing RF circuits [2]-[4]. Using this technology, an earlier capacitor array design, shown in Figs. 1-a and 1-b, demonstrated excellent RF performance [5]. The plates of the array snap down one-by-one, theoretically. However, this capacitor array needed improvements for the following reasons. Fig. 2a shows the effect of the variation in bond height on the capacitive performance. In addition, because the stand-offs were not initially in contact with the substrate, the capacitive plates were forced to bend before pull-in. Finally, only 11% of the area of this 30-plate 1-dimensional (1-D) array was related to the capacitance change. Another design option for a 1-D variable capacitor array is the fixed-fixed beam, shown in Fig. 2b. However, this design also has disadvantages. For example, capacitance values can vary from plate to plate due to warpage caused by a coefficient of thermal expansion (CTE) mismatch. The digital increments in capacitance could also be lost due to uncontrollable pull-in voltages.

The five problems listed above are eliminated in the 2-D MEMS variable capacitor array presented in this work and shown in Fig. 1-c. To improve this variable MEMS capacitor 1-D array, we have developed a 2-D array with a substantial reduction in device area (see Fig. 1-c). The overall device area has been reduced from 0.5mm^2 to 0.19mm^2, while the capacitance related area has increased from 0.055 mm^2 to 0.120 mm^2. In addition, we have developed a post-enabled precision flip-chip assembly process for this 2-D array. Because of precise gap control, the warpage was reduced. Outstanding digital behavior is critical to assure superior RF performance under manufacturing variations.

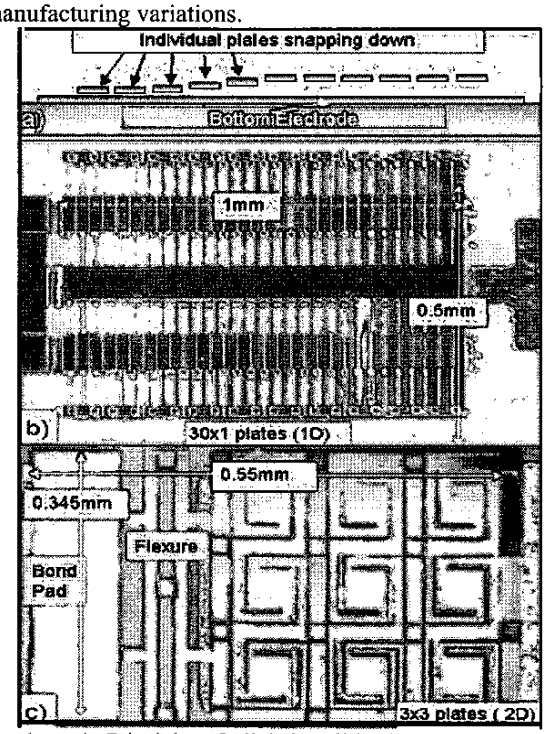

Fig. 1 a) Principle of digital pull-in in MEMS variable capacitors. b) 2-terminal Hoivik MEMS variable capacitor c) New 2-D 3x3 MEMS variable capacitor on 50Ω microstrip transmission line.

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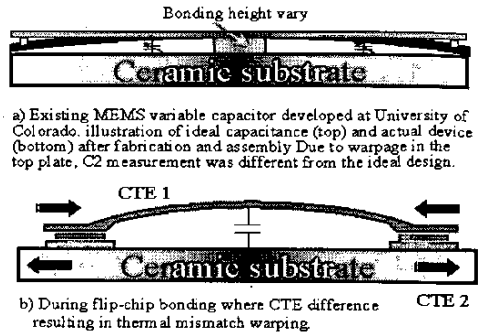

Fig. 2 Existing flip-chip problems: a) The cantilever beam type suffers from variation of bond height and initial bending from short stand offs. b) The fixed-fixed beam suffers from warpage due to a CTE mismatch.

II "POST-ENABLED" FLIP-CHIP ASSEMBLY

a) Flip Chip assembly

The 2-D MEMS variable capacitor array is assembled using flip-chip bonding with tethers on the donor substrate [6] and is illustrated in Fig. 3. The receiving substrate contains microstrip transmission lines consisting of 2.4μm thick gold and 2μm indium bumps. In addition, a 160 nm-thick Alumina layer is deposited by atomic layer deposition (ALD) coating techniques [7] to prevent electrode shorting on pull-in. Before bonding, the MEMS chip is released in 49% hydrofluoric acid (HF) followed by a CO_2 critical-point drying process. The MEMS-based variable capacitor array (M-VCA) is still connected to the silicon substrate by *tethers*. These tethers are then broken during the bonding process, leaving behind the top plate of the M-VCA.

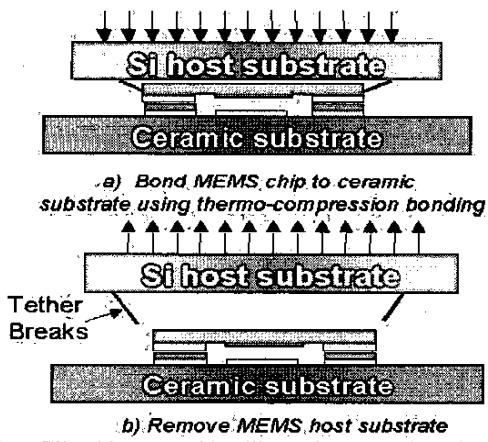

Fig. 3. Flip-chip assembly illustrations. Notice the tether breaks on the sides of the remaining device.

b) Final Assembled device

The 3x3 M-VCA flip-chip assembled device on its ceramic substrate is shown in Fig. 1-c and a side view schematic is provided in Fig. 4. The side-view illustrates how the capacitor plates maintain a uniform air gap with the substrate. Such a gap is achieved by the use of posts, which are critical to the precision flip-chip assembly process. In addition to maintaining a uniform air gap, the posts carry the vertical load during electrostatic actuation. As a result, we were able to use the compliant flexures necessary to accommodate the thermal mismatch between the silicon MEMS and the alumina substrate. The post and plate layer is illustrated in Fig. 5.

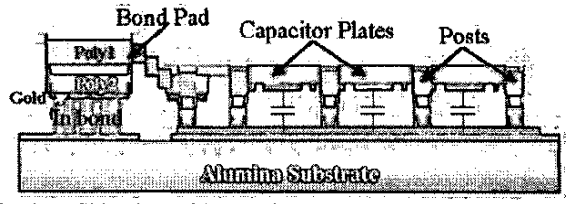

Fig. 4 Side-view of 3 capacitor plates in the up position after flip-chip assembly.

c) Post and Layer structure

Because of the limitations of using just the two structural layers available in the commercial MUMPs process, a novel approach to overcoming the problems in the 1-D array has been conceived, consisting of using four "posts" (legs) designed to hold two plate-flexures carrying the top plate of the capacitor.

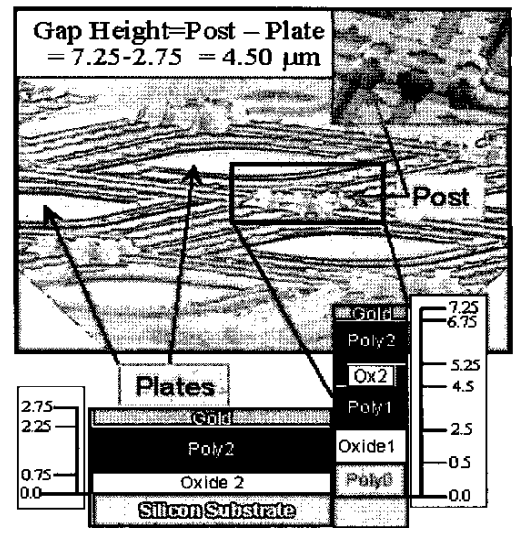

Fig. 5 Posts and plates before the flip-chip assembly

An example of a post's fabrication scheme is shown in Fig. 5. The difference between the height of the post -

which is made of poly0 (0.5 μm), poly1 (2 μm), oxide 2 (0.75 μm), poly2 (1.5 μm) and gold (0.5 μm) - and the height of the plate - which is made of Poly2 (1.5 μm), gold (0.5 μm) and anchor1 (to remove oxide 1 layer) - is 4.5 μm. Other gap heights can also be created using different layer combinations for the posts and plates, three of which are listed in Table 1. Overall, we designed and tested 43 different post-plate configurations, which resulted in 18 different gap heights ranging from 0.25μm to 4.50 μm with 0.25 increments. Having more than one configuration for each gap height is important because material properties like conductivity vary from one layer to the next. Thus, the availability of multiple configurations could allow a device to be better tailored toward a specific application. A SEM image of an array with a uniform gap height is shown in Fig. 6.

Table1
POST AND PLATE LAYER STRUCTURE

Gap (μm)	Plate layers	Post Layers
1.00	P0, P2, gold	P0, P1, P2, via
2.50	P0, P2, anchor1,gold	P1, P2, via
4.50	P2, via, gold	P0, P1, P2, via, gold

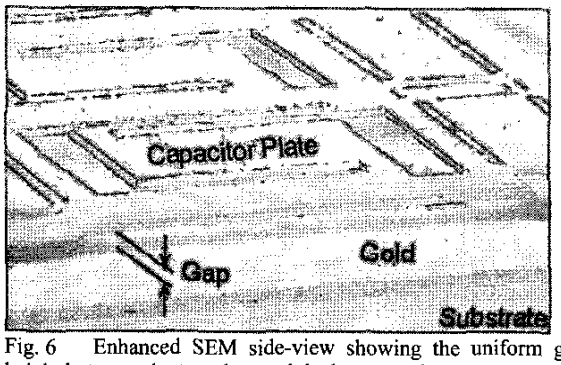

Fig. 6 Enhanced SEM side-view showing the uniform gap height between the top plate and the bottom substrate.

III. RF CHARACTERIZATIONS

The theoretical capacitance, tuning range and Q-factor of the 3x3 M-VCA, shown in Fig. 1-c, were characterized.

a) Calculation of C_{up}

Because of the precision flip-chip assembly, we have achieved good agreement between the theoretical and measured results. Using the parallel-plate capacitance formula ($C_{up}=\varepsilon_o.\varepsilon_r A/d$), which involves the area ($A=345x345\ \mu m^2$) of 9 plates, the relative dielectric for air ($\varepsilon_r=1$), and the gap height ($d=2.75\ \mu m$) between the plates, a theoretical value of C_{up} was obtained as 0.38 pF. This value compares well with the measured value of 0.35 pF (average).

b) CV relationship and tuning ratio

An LCR Meter (Agilent 4263B) with an External Voltage Bias fixture (Agilent 16065A) was used for capacitance measurements at 10KHz. The maximum capacitance, measured at 74 volts with three plates snapped down, was C_{down}= 1.5pF, as seen in Fig. 7. With more plates snapped down, the capacitance would be further increased. At present, the applied voltage is limited to the breakdown voltage of the dielectric coating on the substrate. In addition, the digital increments of the capacitance are clearly shown in Fig. 7. The loss of the digital increments in the previous 1-D array described in the Introduction was eliminated by the use of the precision flip-chip assembly process and its associated device components. Such digital performance can tolerate large manufacturing variation such as the thickness or width variation of the plates.

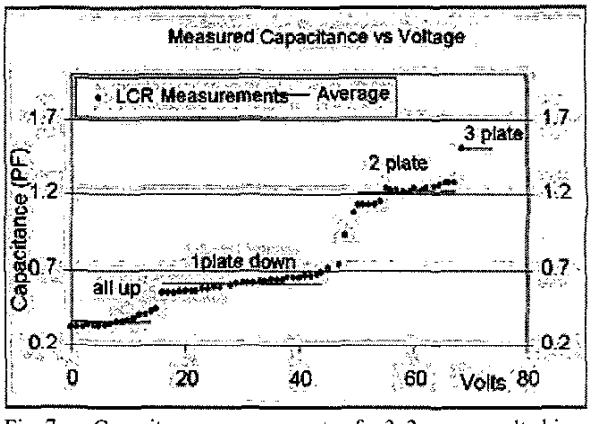

Fig. 7 Capacitance measurements of a 3x3 array resulted in a tuning range of 4.7:1, achieved between 0.32pF and 1.5 pF.

c) Q-factor

We used an HP 8510B Network Analyzer connected to a resonator to measure the Q-factor. This resonator consisted of a coaxial line with rectangular outer conductor and circular inner conductor. The Q-factor of the resonator was very high to allow estimation of the high-Q of the M-VCA. The resonance frequency without the MEMS capacitor was designed to be 1.0 GHz. Fig. 8 shows the resonance curves at various bias voltages and the equivalent circuit. The 150 pF chip capacitor provided a ground path for the RF signal, and the 10 KΩ resistor acted as an RF choke on the bias line. The Q factor for this unloaded circuit was measured to be 240 at 1.05 GHz.

The Q of the MEMS capacitor was calculated using the equation $Q_{mems}=(1/Q_{Load}-1/Q_{unload})^{-1}$, where Q_{Load} and

Q_{unload} were the measured values of the resonator with and without the MEMS device respectively. The Q-factor was measured using the –3dB point method. Since the unloaded Q-factor measured around 240 and the loaded Q factor was measured as 135, the estimation of Q based on the above equation is not very accurate. However the Q-value is certainly in the range of the Q of the unloaded resonator (around 240). This is a major improvement compared with the earlier work [5].

In Fig. 8, the shift in the frequency as a function of voltage is also shown. When voltage was applied, the capacitor plates snapped down one by one to cause the shift of frequency. This figure depicts the actual measurement from the network analyzer.

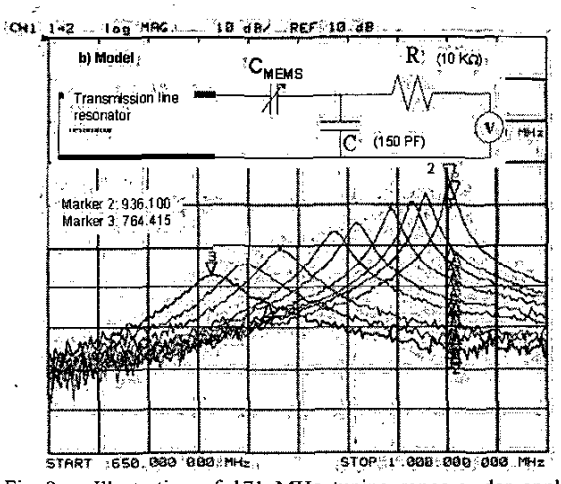

Fig. 8 Illustration of 171 MHz tuning range under applied voltage and equivalent circuit model. Markers 2 and 3 indicate the resonance peaks with 0V and 74V applied respectively.

IV. Conclusion

In conclusion, we have developed a new MEMS-based variable capacitor array. In contrast to the previous work by our group, this new variable capacitor array used a unique post-enabled flip-chip assembly process to achieve excellent mechanical performance, which resulted in excellent RF performance. Table 2 compares the previously published work on a 1-D array with this new 2-D array. The new array increases the Q-factor and tuning ratio while using desirable digital capacitance increments. By design, post-enabled flip-chip bonding can create 18 different gap heights ranging from 0.25 μm to 4.75 μm in 0.25 increments. This novel approach and new variable capacitor array will advance RF-MEMS technology toward large-scale, cost-effective manufacturing.

TABLE 2
COMPARISON BETWEEN PREVIOUS AND CURRENT WORK

RF Comparison	**Hoivik et al (2001)**	**This Work (2002)**
Tuning Ratio	3:1	4.7:1
Q-Factor	140 at 745 MHz	>200 at 936 MHz
Capacitance	Continuous	Digital steps
Integration with RF circuit	2-terminal device	Mounted on CPW, Microstrip, 2-terminals
Mechanical Comparison		
Array Type	30x1 (1D)	3x3 (2D)
Overall size	0.5 mm x 1.0mm	0.345mmx 0.55mm
Space used for capacitance ratio	11%	63%
Gap Height	~2μm	2-4.75 as designed

Acknowledgement

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